region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd- numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction;

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in said second region, in an order corresponding to the order of said even-numbered scanning lines, said even-numbered output pads, driver circuits and selection circuits are arranged as columns in said first direction, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines being arranged in the same row in said second direction;

wherein said integrated circuit includes:

a transfer clock generator that divides the fundamental clock signal that defines the cycle of line-sequential scanning in half,

and a shift data generator that generates said first and second shift data in two consecutive cycles of said fundamental clock signal corresponding to the start pulse that indicates the timing of the start of a frame.

For claim 8:

8. A type of integrated circuit for scan driving for sequentially supplying scan drive signal to the scanning electrodes of a display device; comprising:

a first shift register, which has plural register circuits connected in series, and

a phase opposite to that of said first transfer clock signal; and, by means of the output signals of the flip-flops with said second shift data latched in them, the corresponding driver circuits are selected.

For claim 2: Cancel claim.

For claim 3:

3. The integrated circuit for scan driving as in Claim [[2]]1 wherein said first and second shift registers allow bidirectional transfer of, respectively, said first and second shift data.

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For claim 4:

4. An integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction, plural drive circuits for driving said scanning lines to the active state through said output pads, respectively, and plural selection circuits for individually selecting said driver circuits in a line-sequential scanning cycle in an order corresponding to the order of said scanning lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

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Authorization for this examiner's amendment was given in a telephone interview with attorney William Kempler on 12/18/09.

The application has been amended as follows:

For claim 1:

An integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction, plural drive circuits for driving said scanning lines to the active state through said output pads, respectively, and plural selection circuits for individually selecting said driver circuits in a line-sequential scanning cycle in an order corresponding to the order of said scanning lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second